Amendments to the Specification:

Added text is underlined and deleted text is struck through.

Please replace the section beginning on page 3, line 15 and ending on line 30 with the following:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top plan view of a non-volatile memory transistor device in accordance with the invention.

Fig. 2 is a side sectional view of the device of Fig. 1 taken along lines 2-2.

Fig. 3 is a top plan view of a first read-only memory transistor device in accordance with the invention.

Fig. 4 is a side sectional view of the device of Fig. 3 taken along lines 4-4.

Fig. 5 is a top plan view of a second read-only memory transistor device in accordance with the invention.

Fig. 6 is a side sectional view of the device of Fig. 5 taken along lines 6-6.

Fig. 7 is a schematic diagram of memory cells in a memory array.

Please replace paragraph beginning on page 4, line 3 and ending on line 10 with the following:

A p-type wafer has memory cells ~~that~~ as shown in Fig. 7. Returning to Figs. 1 and 2, the memory cells are laid out by first establishing an active area 11, indicated by stippling in Fig. 1 and defined by a mask. The active area is seen to have longitudinal or lengthwise axis, parallel to line L, but running through the entire length of the active area. The active area is lightly doped and will contain source and drain implants for two MOS transistors.

Please replace paragraph beginning on page 7, line 3 and ending on line 14 with the following:

In operation, it is necessary to separate rows of ROM memory from EEPROM memory in a group. For example, in Fig. 7, some of the rows 12, 14, 16, 18 could form a first group. Columns 22, 24, 26, 28 intersect the rows to form the array. Memory cells such as memory cell 32 reside at the intersections. For such rows, the poly II control gate 43 is tied low to keep the "zero" cells turned off. While most transistors in an array will be ROM memory transistors, several rows of EEPROM memory elements, i.e. a second group of rows, not in the first group can be provided. Within each row of ROM cells, the programming of ones and zeros may be intermixed. Since the footprint for all devices is the same, different memory chips can have a different configuration of read-only memory elements, yet the chip topology will be the same.